Workshop on Component-to-System Level Packaging – Addressing Integration Challenges for Automotive and Industrial Applications

Organized by: Global Electronics Association, IPC by Global Electronics Association, Forschungsfabrik Mikroelektronik Deutschland, APECS European Chiplet Innovation

GEA/IPC supported by Research Fab Microelectronics Germany (FMD) with focus on APECS Pilot Line

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Mercure Hotel MOA Berlin, Stephanstraße 41, 10559 Berlin, Germany

Sponsored by: ASE, Heller Industries, AT&S, Kim Young Europe, RESONAC Chemistry for Change

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The road to autonomous driving and the need for more electrified mobility have resulted in sizable changes for electronics such as semiconductors and batteries used in automotive applications. Smart homes and infrastructure, factory automation and preventive maintenance have driven significant advancements in industrial electronics too.

These applications demand significant system miniaturization through complex chiplet concepts and heterogenous integration solutions for processors, memories, power management along with sensors and MEMS, wireless and optical connectivity and other advanced communication components and systems.

Though assembly levels 0 and 1, with chip-package interaction challenges addressed, packaged device/components formation is enabled. Assembly levels 2 and 3 (board and system assembly) are indispensable from system level integration and final product/system performance points of view. With heterogenous integration solutions and miniaturization, the board as we know it today is partially moving inside the package, and System-in-Package (SiP) is created.

Advancements in compute and storage for automotive applications, sensor technologies with mmWave Radar, LIDAR, and other sensing techniques along with integrated power systems for EV with high voltage, high power components and modules are bringing new challenges to both, Component-Level Packaging (CLP) and Board/System-Level-Packaging (SLP). Power delivery, thermal management, assembly and reliability at component/system level demand innovative design approaches, materials and assembly processes for high reliability automotive and industrial requirements.

BE PART OF THE SOLUTION - The workshop is intended to bring together industry experts presenting and discussing CLP and SLP trends, requirements, challenges, solutions and the needs for guidelines/ standards desired for design, assembly, test, reliability and manufacturing from components (OSAT) and electronic manufacturing solutions (EMS) perspective.

PLANNED OUTCOME - To initiate pre-competitive project proposals, which could be funded Research and Innovation Actions (RIA) or Innovation Actions (IA) industry projects, preferably in connection with the APECS pilot line.

Confirmed Speakers + Panelists along the supply chain (status 06/30/2025)**:**

ASE, AT&S, Continental, EPoSS, Forschungsfabrik Mikroelektronik Deutschland, Fraunhofer IIS, Fraunhofer IZM, Indium Corporation, Infineon, Global Electronics Association, IPC by Global Electronics Association, Kitron, neways, NXP, RESONAC Chemistry for Change, SIEMENS, swissbit, Würth Elektronik